REMARKS

Applicant has reviewed and considered the Office Action mailed on September 17, 2003, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 10, 11, 13-18, 20-24, 26-38, and 40-45 are now pending in this application.

First §103 Rejection of the Claims

Claims 10, 11, 13-18, 20-24, 26, 27, 29-38, 44, and 45 were rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. 5,982,690) in view of Chung (U.S. 5,442,209) and Hidaka (U.S. 6,459,301). Applicant traverses these grounds for rejection. Further, Applicant reserves the right to swear behind Austin and Hidaka at a later date.

The Office Action stated

> "Applicant argues that non of the prior art that teach the size of the dual gate transistor is ranging about 0.3V to 0.35V and the sense amplifier circuit is able to output a full output sense voltage in less than 10 ns. The examiner respectfully disagrees. Hadika teaches that by reducing the supply voltage and the threshold of each transistors, a circuit can operate in high speed and reduce its power consumption. One skill in the art would have been motivate to select the threshold of the dual gate transistors to be ranging from 0.3V to 0.35V in order to increase the speed of the circuit. Furthermore, with proper selection for the threshold of the transistors, the circuit will be able to output a full output sense voltage less than 10ns because the circuit will achieve a high speed operation when the supply voltage the threshold each of the transistors in the circuit are reduced."

Applicant directs the Examiners attention to column 1, lines 32-45, of Hidaka referenced by the Office Action. The above quote from the Office Action does not include the additional information provided by Hidaka on lines 38-42: "In this case, a subthreshold current flowing between a source and a drain when the transistor is in the off state increases. This increases a direct current in the entire large scale integration and especially increases a standby current in a dynamic semiconductor memory device." Thus, Hidaka indicates that the reduced supply voltage and threshold do not lead to overall reduction in power consumption. Austin deals with the problem of circuits with excessive current and power consumption. *See, Austin column 1, lines 39-49.* Austin further deals with a memory device that draws little static current. *See,*

Austin column 2, lines 44-45. Applicant respectfully submits that combining Hidaka with Austin as proposed in the Office Action would be contrary to Austin's purpose of drawing little static current. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); MPEP § 2143.01.

Additionally, the Hidaka general statement "the threshold of each MOS transistor needs to be lowered in accordance with the decreased supply voltage," *(See, Austin column 1, lines 36-38)* in the Hidaka section referenced in the Office Action is indefinite. The Office Action does not provide any reference teaching or disclosing a dual-gated MOSFET having a threshold voltage ranging from about 0.3 to about 0.35 range or a circuit providing a full output voltage in less than 10 ns. The general statement quoted above from the reference section does not teach or suggest the elements from the instant independent claims that are void from the Austin and Chung references. The attribution provided by the Office Action that "[o]ne skill in the art would have been motivate to select the threshold of the dual gate transistors to be ranging from 0.3V to 0.35V in order to increase the speed of the circuit. Furthermore, with proper selection for the threshold of the transistors, the circuit will be able to output a full output sense voltage less than 10ns because the circuit will achieve a high speed operation when the supply voltage the threshold each of the transistors in the circuit are reduced" is a conclusionary that has not been supported by objective evidence or a reference other than Applicant's disclosure. Since no reference has bee provided for this statement with respect to the threshold voltages ranging from about 0.3V to about 0.35V for a dual-gated MOSFET and with respect to a circuit having a dual-gated MOSFET outputting a full output voltage in less than 10 ns, Applicant requests the Examiner to provide a reference that describes such elements. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

From the discussion above, Applicant respectively submits that the proposed combination of Hidaka with Austin in the Office Action is not proper. Even if combined, Applicant can not find in Austin or in Chung or in Hidaka a teaching or suggestion of a dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V, as recited in independent

claim 10, and Applicant can not find in Austin or in Chung or in Hidaka a teaching or suggestion of a circuit having dual-gated MOSFET, where the circuit can output a full output voltage in less than 10 ns, as recited in independent claim 16. Thus, Austin in view of Chung in further view of Hidaka does not teach or suggest all the elements as recited in claim 10 and Austin in view of Chung in further view of Hidaka does not teach or suggest all the elements as recited in claim 16. Thus, the cited references do not establish a proper *prima facie* case of obviousness with respect to claims 10 and 16 and that claims 10 and 16 are patentable over Austin in view of Chung in further view of Hidaka.

Claims 17, 23, 29, 32, 33, 37, 40, 44, and 45 recite similar elements as claim 10 and are patentable over Austin in view of Chung in further view of Hidaka for the reasons stated above and additionally in view of the further elements recited in these independent claims. Additionally, claims 22 and 31 recite similar elements as claim 16 and are patentable over Austin in view of Chung in further view of Hidaka for the reasons stated above and additionally in view of the further elements recited in these independent claims.

Claims 11, 13, and 14, claims 18, and 20-21, claims 24 and 26-28, claim 30, claims 34-36, claim 38, and claims 41-43 are dependent on claims 10, 17, 23, 29, 33, 37, and 40, respectively, and are patentable over Austin in view of Chung for the reasons stated above and additionally in view of the further elements recited in these dependent claims.

Applicant respectively requests withdrawal of these rejections to claims 10, 11, 13, 14, 16-18, 20-24, 26, 27, 29-38 & 44-45, and reconsideration and allowance of these claims.

Second §103 Rejection of the Claims

Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (U.S. 6,069,828) in view of Austin (U.S. 5,982,690), Hidaka (U.S. 6,459,301), and Chung (U.S. 5,442,209). Applicant traverses these grounds for rejection. Further, Applicant reserves the right to swear behind Austin and Hidaka at a later date.

Claim 28 is dependent on claim 23, where claim 23 recites a "dual-gated NMOS having a threshold voltage ranging from about 0.3 V to about 0.35V." Applicant can not find in Austin or in Hidaka or a teaching or suggestion of a dual-gated NMOS transistor as recited in claims 23 and 28. Chung deals with reducing the number of connections between neurons in a neutral

network by using transistors that have a common drain and common source. Applicant can not find or in Chung a teaching or suggestion of a dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V as recited in claims 23 and 28. Therefore, Chung does not cure the abovementioned deficiencies of Austin and Hidaka.

The Office Action applies Kaneko et al. (hereafter Kaneko) noting that Kaneko "shows all elements of the claim except for the detail of the sense amplifier." Therefore, Kaneko also does not cure the deficiencies of Austin. Thus, Austin in view of Chung, Hidaka, and Kaneko does not teach or suggest all the elements of claim 28.

Claim 40 recites "dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V." As stated above, Kaneko does not cure the abovementioned deficiencies of Austin, Hidaka, and Chung. Thus, Austin in view of Chung, Hidaka, and Kaneko does not teach or suggest all the elements of claim 40.

Claims 41-43 are dependent on claim 40 and are patentable over Kaneko in view of Austin, Chung, and Hidaka, for the reasons stated above and additionally in view of the further elements recited in these dependent claims.

Applicant respectively requests withdrawal of these rejections of claims 28 and 40-43, and reconsideration and allowance of these claims.

Assertion of Pertinence

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2157 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 17 November 2003 By David R. Cochran

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17th day of November, 2003.

Amy Moriarty
Name

Signature